XRD9855/9856
XRD98L55/98L56

CCD Image Digitizers with
CDS, PGA and 10-Bit A/D

July 2001

FEATURES

- 10-Bit Resolution ADC
- 18 - 27MHz Maximum Sampling Rate
- Correlated Double Sampling (CDS)
- Programmable Gain from 6dB to 38dB (PGA)
- Digitally Controlled Analog Offset-Calibration
- CCD Black Level Offset Compensation at Frame Rate
- CDS Clocks Sample Rising Edge or Falling Edge
- Single 5V or 3V Power Supply
- Low Power for Battery Applications:
  XRD9855/56: 250/300mW @ V_{DD} = 5.0V
  XRD98L55/L56: 120/150mW @ V_{DD} = 3.0V
- 50µA-Typ Current in Stand By Mode
- 3-State Digital Outputs
- ESD Protection to Over 2000V

APPLICATIONS

- Digital Video Camcorders
- Digital Still Cameras
- PC Video Teleconferencing
- Digital Copiers
- Infrared Image Digitizers
- CCD/CIS Imager Interface
- CCTV/Security Camera
- 2D Bar Code Readers
- Industrial Cameras

GENERAL DESCRIPTION

The XRD9855/XRD9856 are complete CCD Image Digitizers for digital cameras. The products include a high bandwidth differential Correlated Double Sampler (CDS), 8-bit digitally Programmable Gain Amplifier (PGA), 10-bit Analog-to-Digital Converter (ADC) and digital controlled black level auto-calibration circuitry.

The Correlated Double Sampler (CDS) subtracts the CCD output signal black level from the video level. Common mode signal noise and power supply noise are rejected by the differential CDS input stage. CDS inputs are designed to be used either differential or single-ended.

The auto calibration circuit compensates for any internal offset of the XRD9855/XRD9856 as well as black level offset from the CCD.

The PGA is digitally controlled with 8-bit resolution on a linear dB scale, resulting in a gain range of 6dB to 38dB with 0.125dB per LSB of the gain code.

The PGA and black level auto-calibration are controlled through a simple 3-wire serial interface. The timing circuitry is designed to enable users to select a wide variety of available CCD and image sensors for their applications.

The XRD9855/XRD9856 has direct access to the PGA output and ADC input through the pin TESTVIN.

The XRD9855/XRD9856 are packaged in 48-lead surface mount TQFP to reduce space and weight, and suitable for hand-held and portable applications.

ORDERING INFORMATION

Part No.	Package	Temperature Range	Operating Power Supply	Maximum Sampling Rate
XRD9855AIV	48 Lead TQFP (7 x 7 x 1.4 mm)	-40°C to 85°C	5.0V	18 MSPS
XRD98L55AIV	48 Lead TQFP (7 x 7 x 1.4 mm)	-40°C to 85°C	3.0V	18 MSPS
XRD9856AIV	48 Lead TQFP (7 x 7 x 1.4 mm)	-40°C to 85°C	5.0V	27 MSPS
XRD98L56AIV	48 Lead TQFP (7 x 7 x 1.4 mm)	-40°C to 85°C	3.0V	27 MSPS

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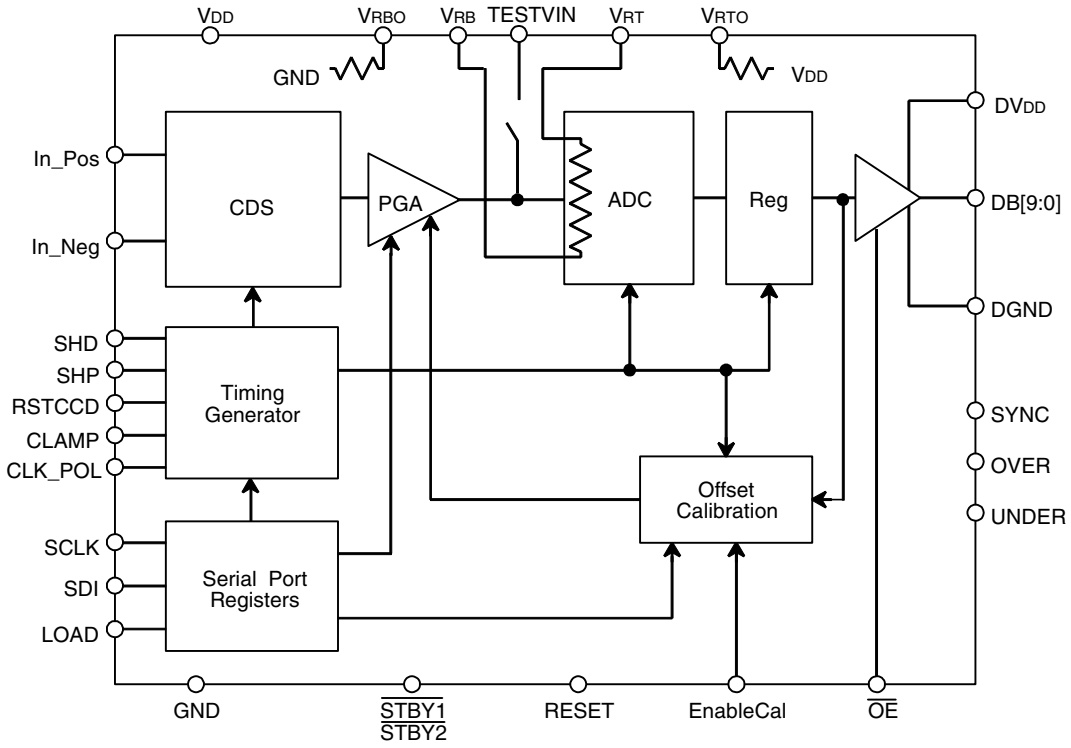
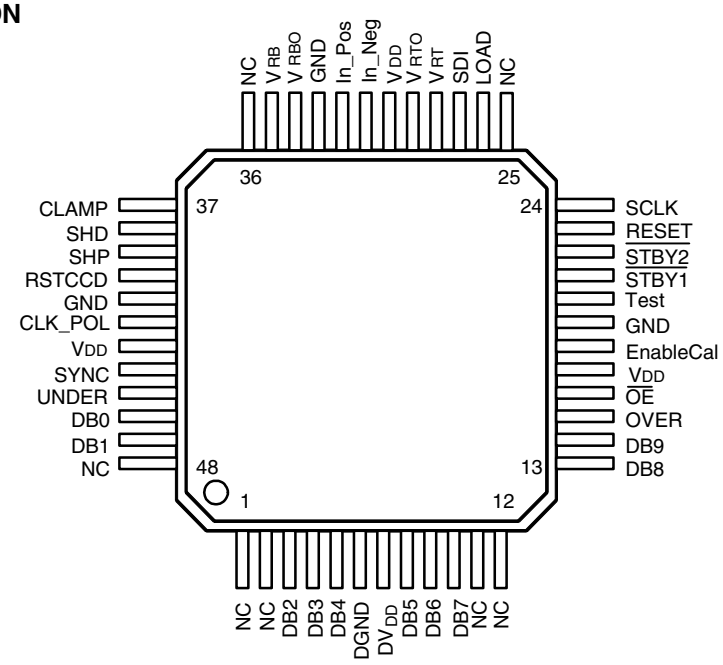


Figure 1. XRD9855/XRD9856 Simplified Block Diagram

PIN CONFIGURATION



48 Lead TQFP (7 x 7 x 1.0 mm)

PIN DESCRIPTION – 48 pin TQFP

Pin #	Symbol	Description
1	NC	**No Connect.**
2	NC	**No Connect.**
3	DB2	**ADC Output.** DB0 is the LSB, DB9 is the MSB.
4	DB3	**ADC Output.**
5	DB4	**ADC Output.**
6	DGND	**Digital Output Ground.**
7	DV_{DD}	**Digital Output Power Supply.** Must be less than or equal to V_{DD}.
8	DB5	**ADC Output.**
9	DB6	**ADC Output.**
10	DB7	**ADC Output.**
11	NC	**No Connect.**
12	NC	**No Connect.**
13	DB8	**ADC Output.**
14	DB9	**ADC Output.** MSB
15	OVER	**Over Range Output Bit.** OVER goes high to indicate the ADC input voltage is greater than V_{RT}.

PIN DESCRIPTION – 48 pin TQFP (CONT'D)

Pin #	Symbol	Description
16	$\overline{OE}$	**Digital Output Enable (Three-State Control).** Pull $\overline{OE}$ low to enable output drivers. Pull $\overline{OE}$ high to put output drivers in high impedance state.
17	V_{DD}	**Analog Power Supply.**
18	EnableCal	**Calibration Enable.** Automatic offset calibration control.
19	GND	**Analog Ground.**
20	TESTVIN	**ADC Test Input & PGA Test Output.**
21	$\overline{STBY1}$	**Standby Control 1.** Pull low to put chip in power down mode.
22	$\overline{STBY2}$	**Standby Control 2.** Short to $\overline{STBY1}$ pin if not using TESTVIN pin.
23	RESET	**Chip Reset.** Pull high to reset all internal registers.
24	SCLK	**Shift Clock.** Shift register latches SDI data on rising edges of SCLK.
25	NC	**No Connect.**
26	LOAD	**Data Load.** Rising edge loads data from shift register to internal register. Load must be low to enable shift register.
27	SDI	**Serial Data Input.**
28	V_{RT}	**Top ADC Reference.** Voltage at V_{RT} sets full-scale of ADC.
29	V_{RTO}	**Internal Bias for V_{RT}.** Short V_{RT} to V_{RTO} to use internal reference voltage.
30	V_{DD}	**Analog Power Supply.**
31	In_Neg	**CDS Inverting Input.** Connect via capacitor to CCD video output.
32	In_Pos	**CDS Non-inverting Input.** Connect via capacitor to CCD supply.
33	GND	**Analog Ground.**
34	V_{RBO}	**Internal Bias for V_{RB}.** Short V_{RB} to V_{RB0} to use internal reference voltage.
35	V_{RB}	**Bottom ADC Reference.** Voltage at V_{RB} sets zero scale of the ADC.
36	NC	**No Connect.**
37	CLAMP	**CDS DC Restore Clamp.** Clamps In_Pos & In_Neg to internal bias voltage.
38	SHD	**CDS Clock.** Controls sampling of the pixel video level.
39	SHP	**CDS Clock.** Controls sampling of the pixel black level.
40	RSTCCD	**CCD Reset Pulse Disconnect.** Used to decouple CDS during the reset pulse.
41	GND	**Analog Ground.**
42	CLK_POL	**Clock Polarity.** Controls the polarity of SHP, SHD & CLAMP.
43	V_{DD}	**Analog Power Supply.**
44	SYNC	Digital output for Exar test purposes only. **No connect.**
45	UNDER	**Under Range Output Bit.** UNDER goes high to indicate the ADC input voltage is less than V_{RB}.
46	DBO	**ADC Output.** LSB
47	DB1	**ADC Output**.
48	NC	**No Connect.**

DC ELECTRICAL CHARACTERISTICS – XRD9855 and XRD9856
Unless otherwise specified: $DV_{DD} = V_{DD} = 5.0V$, **Pixel Rate = 18MSPS,** $V_{RT} = 3.8V$, $V_{RB} = 0.5V$

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
CDS Performance						
$CDSV_{IN}$	Input Range		200	800	mV_{PP}	Pixel (Black Level - Video Level)
BW	Small Signal Bandwidth (-3dB)		60		MHz	
SR	Slew Rate		40		V/µs	400mV Step Input
FT	Feed–through (Hold Mode)		-60		dB	
PGA Parameters						
AV_{MIN}	Minimum Gain	3.5	5	6.5	dB	
AV_{MAX}	Maximum Gain	35.5	37	38.5	dB	
PGA n	Resolution		8		bits	Transfer function is linear steps in dB (1LSB = 0.125dB)
GE	Gain Error		5		% FS	At maximum or minimum gain setting
ADC Parameters (Measured Through TESTVIN)						
ADC n	Resolution	10			bits	
f_s	Max Sample Rate	27			MSPS	
DNL	Differential Non-Linearity	-1	±0.75	1.2	LSB	Up to 18MHz sample rate (XRD9855)
DNL27	Differential Non-Linearity	-1	±1.3	2.0	LSB	Up to 27MHz sample rate (XRD9856)
EZS	Zero Scale Error	-50		50	mV	Measured relative to V_{RB}
EFS	Full Scale Error			4	% FS	
V_{IN}	DC Input Range	GND		V_{DD}	V	V_{IN} of the ADC can swing from GND to V_{DD}. Input range is limited by the output swing of the PGA
V_{RT}	Top Reference Voltage	1.5	3.8	V_{DD}	V	$V_{RT} > V_{RB}$
V_{RB}	Bottom Reference Voltage	0.3	0.5	V_{DD}-1	V	$V_{RT} > V_{RB}$
ΔV_{REF}	Differential Reference Voltage	1.0	3.3	V_{DD}	V	
R_L	Ladder Resistance	280	400	520	Ohms	
V_{RB}	Self Bias V_{RB} $\left(V_{RB} = \frac{V_{DD}}{10}\right)$	0.4	0.5	0.6	V	V_{RB} connected to V_{RBO}
V_{RT}	Self Bias V_{RT} $\left(V_{RT} = \frac{V_{DD}}{1.30}\right)$	3.5	3.8	4.1	V	V_{RT} connected to V_{RTO}

DC ELECTRICAL CHARACTERISTICS – XRD9855 and XRD9856 (CONT'D)
Unless otherwise specified: DV_{DD} = V_{DD} = 5.0V, Pixel Rate = 18MSPS, V_{RT} = 3.8V, V_{RB} = 0.5V

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
System Specifications						
DNL_S	System DNL		1.0		LSB	XRD9855 up to 18 MSPS
DNL_{S27}	System DNL 27 MSPS		1.0		LSB	XRD9856 up to 27 MSPS
INL_{SMIN}	INL @ Minimum Gain				LSB	INL error is dominated by CDS/PGA linearity.
INL_{SMAX}	INL @ Maximum Gain				LSB	INL error is dominated by CDS/PGA linearity.
$V_{OS\ MINAV}$	Offset (Input Referred) @ Minimum Gain		5		mV	Offset is defined as the input pixel value-0.5 LSB required to cause the ADC output to switch from "Zero scale" to "Zero scale + 1LSB".
$V_{OS\ MAXAV}$	Offset (Input Referred) @ Maximum Gain		1		mV	Offset is measured after calibration. Zero scale is the code in the offset register. Offset depends on PGA gain code.
$en_{\ MAXAV}$	Input Referred Noise @ Maximum Gain		0.2		mV_{rms}	Noise depends upon gain setting of the PGA.
$en_{\ MINAV}$	Input Referred Noise @ Minimum Gain		1.1		mV_{rms}	Noise depends upon gain setting of the PGA.
Digital Inputs						
V_{IH}	Digital Input High Voltage	2.0			V	
V_{IL}	Digital Input Low Voltage			0.7	V	
I_L	DC Leakage Current		5		µA	Input Between GND and V_{DD}.
C_{IN}	Input Capacitance		5		pF	
Digital Outputs						
V_{OH}	Digital Output High Voltage	DV_{DD}-0.5			V	While sourcing 2mA.
V_{OL}	Digital Output Low Voltage			0.5	V	While sinking 2mA.
I_{OZ}	High-Z Leakage	-10		10	µA	$\overline{OE}$=1 or $\overline{STBY1}$= $\overline{STBY2}$ = 0. Output between GND & DV_{DD}.

DC ELECTRICAL CHARACTERISTICS – XRD9855 and XRD9856 (CONT'D)
Unless otherwise specified: $DV_{DD} = V_{DD} = 5.0V$, Pixel Rate = 18MSPS, $V_{RT} = 3.8V$, $V_{RB} = 0.5V$

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
Digital I/O Timing						
T_{DL}	Data Valid Delay		20	25	ns	
T_{PW1}	Pulse Width of SHD	10			ns	
T_{PW2}	Pulse Width of SHD	10			ns	
T_{PIX}	Pixel Period	37	56		ns	
T_{BK}	Sample Black Aperture Delay		6		ns	V_{DD} = 4.5V to 5.5V, Temperature -40°C to 85°C range
T_{VD}	Sample Video Aperture Delay		5		ns	V_{DD} = 4.5V to 5.5V, Temperature -40°C to 85°C range
T_{RST}	RSTCCD Switch Delay	0		4	ns	V_{DD} = 4.5V to 5.5V, Temperature -40°C to 85°C range
T_{SC}	Shift Clock Period	50	100		ns	
T_{SET}	Shift Register Setup Time	10			ns	
Latency	Pipeline Delay			4	cycles	
Power Supplies						
V_{DD}	Analog Supply Voltage	4.5	5.0	5.5	V	
DV_{DD}	Digital Output Supply Voltage	2.7	5.0	5.5	V	$DV_{DD} \leq V_{DD}$ Always
I_{DD}	Supply Current		50	75	mA	$DV_{DD} = V_{DD} = 5.0V$ (XRD9855)
I_{DD27}	Supply Current @ 27MHz		55	85	mA	F_S = 27MHz (XRD9856)
I_{DDPD}	Power Down Supply Current		50	100	µA	$\overline{STBY1}$ = 0 and $\overline{STBY2}$ = 0

DC ELECTRICAL CHARACTERISTICS – XRD98L55 and XRD98L56
Unless otherwise specified: $DV_{DD} = V_{DD} = 2.7V$, Pixel Rate = 18MSPS, $V_{RT} = 2.07V$, $V_{RB} = 0.27V$

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
CDS Performance						
$CDSV_{IN}$	Input Range		200	800	mV_{PP}	Pixel (Black Level - Video Level)
BW	Small Signal Bandwidth (-3dB)		60		MHz	
SR	Slew Rate		40		V/µs	400mV Step Input
FT	Feed-through (Hold Mode)		-60		dB	
PGA Parameters						
AV_{MIN}	Minimum Gain	3.5	5	6.5	dB	
AV_{MAX}	Maximum Gain	36.5	37	38.5	dB	
PGA n	Resolution		8		bits	Transfer function is linear steps in dB (1LSB = 0.125dB)
GE	Gain Error		5		% FS	At maximum or minimum gain setting
ADC Parameters (Measured Through TESTVIN)						
ADC n	Resolution	10			bits	
f_s	Max Sample Rate	27			MSPS	
DNL	Differential Non-Linearity	-1	±0.75	1.2	LSB	Up to 18MHz sample rate (XRD98L55)
DNL27	Differential Non-Linearity	-1	±1.3	2.0	LSB	Up to 27MHz sample rate (XRD98L56)
EZS	Zero Scale Error	-50		50	mV	Measured relative to V_{RB}
EFS	Full Scale Error			4	% FS	
V_{IN}	DC Input Range	GND		V_{DD}	V	V_{IN} of the ADC can swing from GND to V_{DD}. Input range is limited by the output swing of the PGA
V_{RT}	Top Reference Voltage	1.2	2.07	V_{DD}	V	$V_{RT} > V_{RB}$
V_{RB}	Bottom Reference Voltage	0.2	0.27	V_{DD}-1	V	$V_{RT} > V_{RB}$
ΔV_{REF}	Differential Reference Voltage	1.0	1.8	V_{DD}	V	
R_L	Ladder Resistance	280	400	520	Ohms	
V_{RB}	Self Bias V_{RB} $\left(V_{RB} = \frac{V_{DD}}{10}\right)$	0.20	0.30	0.40	V	V_{RB} connected to V_{RBO}
V_{RT}	Self Bias V_{RT} $\left(V_{RT} = \frac{V_{DD}}{1.30}\right)$	2.0	2.3	2.6	V	V_{RT} connected to V_{RTO}. T_{PW2}

DC ELECTRICAL CHARACTERISTICS – XRD98L55 and XRD98L56 (CONT'D)
Unless otherwise specified: DV_{DD} = V_{DD} = 2.7V, Pixel Rate = 18MSPS, V_{RT} = 2.7V, V_{RB} = 0.27V

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
System Specifications						
DNL_S	System DNL		1.0		LSB	XRD98L55 up to 18 MSPS
DNL_{S27}	System DNL 27 MSPS		1.5		LSB	XRD98L56 up to 27 MSPS
INL_{SMIN}	INL @ Minimum Gain		2		LSB	INL error is dominated by CDS/PGA linearity.
INL_{SMAX}	INL @ Maximum Gain		2		LSB	INL error is dominated by CDS/PGA linearity.
$V_{OS\ MINAV}$	Offset (Input Referred) @ Minimum Gain		5		mV	Offset is defined as the input pixel value -0.5 LSB required to cause the ADC output to switch from "Zero scale" to "Zero scale + 1LSB". Offset is measured after calibration.
$V_{OS\ MAXAV}$	Offset (Input Referred) @ Maximum Gain		1		mV	Zero scale is the code in the offset register. Offset depends on PGA gain code.
$en_{\ MAXAV}$	Input Referred Noise @ Maximum Gain		0.2		mV_{rms}	Noise depends upon gain setting of the PGA.
$en_{\ MINAV}$	Input Referred Noise @ Minimum Gain		0.7		mV_{rms}	Noise depends upon gain setting of the PGA.
Digital Inputs						
V_{IH}	Digital Input High Voltage	1.5			V	
V_{IL}	Digital Input Low Voltage			0.7	V	
I_L	DC Leakage Current		5		µA	Input Between GND and V_{DD}.
C_{IN}	Input Capacitance		5		pF	
Digital Outputs						
V_{OH}	Digital Output High Voltage	DV_{DD}-0.5			V	While sourcing 2mA.
V_{OL}	Digital Output Low Voltage			0.5	V	While sinking 2mA.
I_{OZ}	High–Z Leakage	-10		10	µA	$\overline{OE}$=1 or $\overline{STBY1}$= $\overline{STBY2}$ = 0. Output between GND & DV_{DD}.

DC ELECTRICAL CHARACTERISTICS – XRD98L55 and XRD98L56 (CONT'D)
Unless otherwise specified: DV_{DD} = V_{DD} = 2.7V, Pixel Rate = 18MSPS, V_{RT} = 2.07V, V_{RB} = 0.27V

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
Digital I/O Timing						
T_{DL}	Data Valid Delay		28	35	ns	
T_{PW1}	Pulse Width of SHD	10			ns	
T_{PW2}	Pulse Width of SHD	10			ns	
T_{PIX}	Pixel Period	37	56		ns	
T_{BK}	Sample Black Aperture Delay		7		ns	V_{DD} = 2.7V to 3.6V, Temperature -40°C to 85°C range
T_{VD}	Sample Video Aperture Delay		6		ns	V_{DD} = 2.7V to 3.6V, Temperature -40°C to 85°C range
T_{RST}	RSTCCD Switch Delay	0		5	ns	V_{DD} = 2.7V to 3.6V, Temperature -40°C to 85°C range
T_{SC}	Shift Clock Period	50	100		ns	
T_{SET}	Shift Register Setup Time	10			ns	
Latency	Pipeline Delay			4	cycles	
Power Supplies						
V_{DD}	Analog Supply Voltage	2.7	3.0	3.6	V	
DV_{DD}	Digital Output Supply Voltage	2.7	3.0	3.6	V	$DV_{DD} \le V_{DD}$ Always
I_{DD}	Supply Current		40	55	mA	DV_{DD} = V_{DD} = 3.0 V (XRD9855)
I_{DD27}	Supply Current @ 27MHz		45	65	mA	F_S = 27MHz (XRD9856)
I_{DDPD}	Power Down Supply Current		50	100	µA	$\overline{STBY1}$ = 0 and $\overline{STBY2}$ = 0

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2, 3]

V_{DD} to GND ..... +7.0V
V_{RT} & V_{RB} ..... V_{DD} +0.5 to GND -0.5V
V_{IN} ..... V_{DD} +0.5 to GND -0.5V
All Inputs ..... V_{DD} +0.5 to GND -0.5V
All Outputs ..... V_{DD} +0.5 to GND -0.5V
Storage Temperature ..... -65°C to 150°C
Lead Temperature (Soldering 10 seconds) ..... 300°C
Maximum Junction Temperature ..... 150°C
Package Power Dissipation Ratings (T_A= +70°C)
TQFP ..... θ_{JA} = 54°C/W
ESD 2000V

Notes:
1 *Stresses above those listed as "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.*
2 *Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082–2835) from input pin to the supplies. All inputs have protection diodes which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.*
3 *V_{DD} refers to AV_{DD} and DV_{DD}. GND refers to AGND and DGND.*

SYSTEM DESCRIPTION

Correlated Double Sample/Hold (CDS) & Programmable Gain Amplifier (PGA); Gain [7:0]

The function of the CDS block, shown in *Figure 2*, is to sense the voltage difference between the black level and video level for each pixel. The CDS and PGA are fully differential. The PGA output is converted to a single ended signal, and then fed to the ADC. IN_POS (CDS non-inverting input) should be connected, via a capacitor, to the CCD "Common" voltage. This is typically the CCD Reference output or ground. IN_NEG (CDS inverting input) should be connected, via a capacitor, to the CCD output signal.

During the black reference phase of each pixel the SDRK switches are turned on, shorting the PGA1 inputs to V_{DD}. The sampling edge of SHP turns off the SDRK switches, sampling the black reference voltage on capacitors C1 & C2.

During the video phase of each pixel the SPIX switches are turned on. The difference between the pixel reference level and video level is transmitted through capacitors C1 & C2 and converted to a fully differential signal by the differential amplifier PGA1. The sampling edge of SHD turns off the SPIX switches, sampling the pixel value on capacitors C3 & C4.

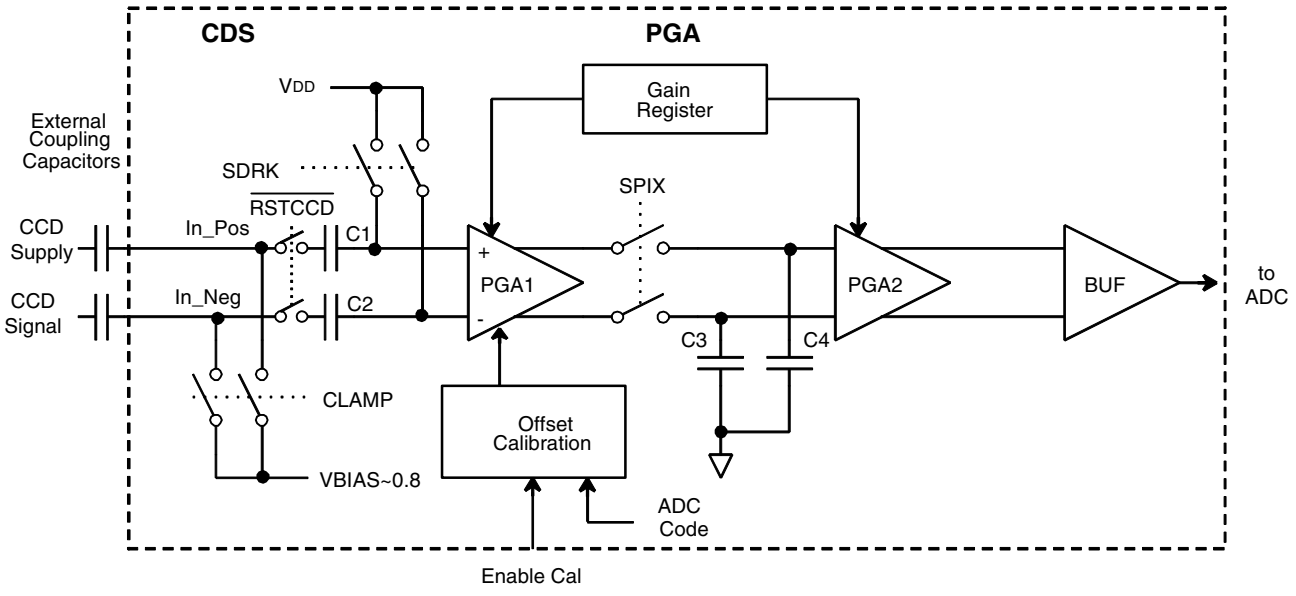


Figure 2. Block Diagram of the CDS & PGA

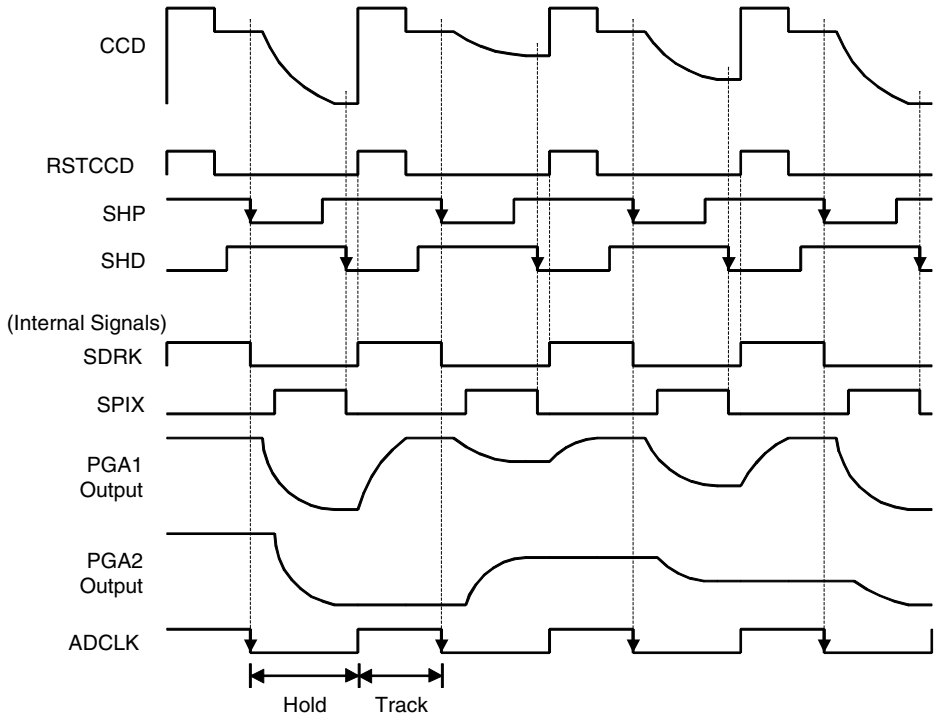


Figure 3. Timing Diagram of the CDS Clocks and Internal Signals, CLK_POL = 1, M2=0

PGA1 provides gains of 0dB, 8dB & 16dB (1x, 2.5x, and 6.25x). The gain transitions occur at PGA gain codes 64d and 128d (40h & 80h). PGA2 provides gain from 6dB to 22dB (2x to 12.5x) with 0.125dB steps. *Figure 4* shows the measured PGA gain vs. Gain Code. The combined PGA blocks provide a programmable gain range of 32dB. The minimum gain (code 00h) is 6dB. The maximum gain (code FFh) is 38dB. The following equation can be used to compute PGA gain from the gain code:

$$Gain[dB] = 6 + \left(32 \times \frac{code}{256}\right)$$

where code is between 0 and 255.
Due to device mismatch the gain steps at codes 63-64 and 127-128 may not be monotonic.

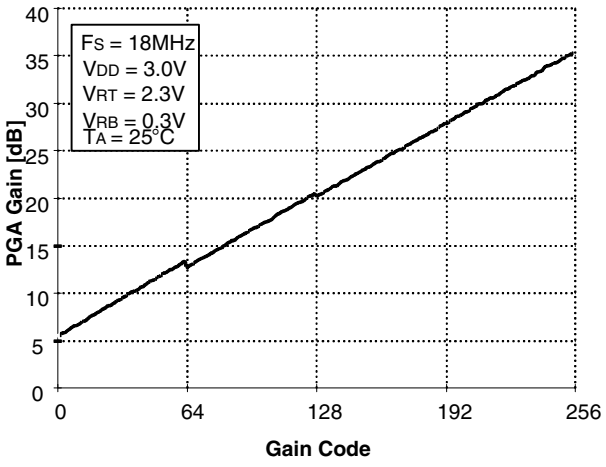


Figure 4. PGA Gain vs. Gain Code

Analog-to-Digital Converter

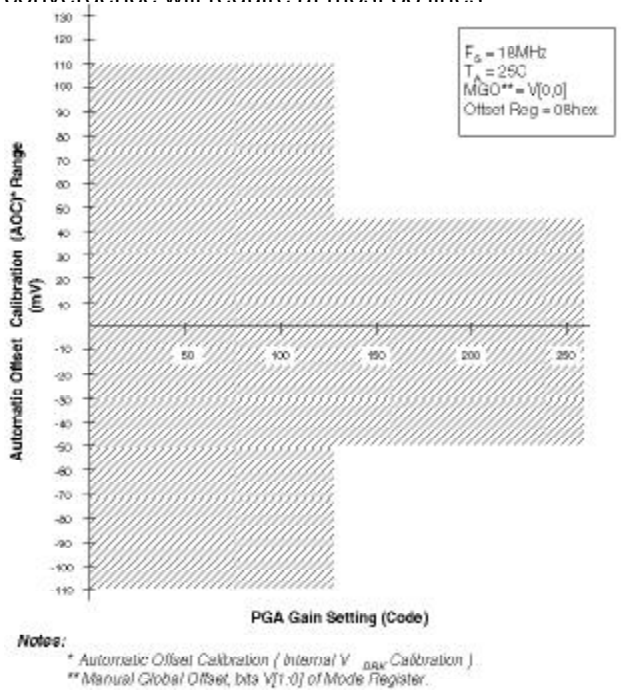
The analog-to-digital converter is based upon a two-step sub-ranging flash converter architecture with a built in track and hold input stage. The ADC conversion is controlled by an internally generated signal, ADCLK (see *Figure 3).* The ADC tracks the output of the CDS/PGA while ADCLK is high and holds when ADCLK is low. This allows maximum time for the CDS/PGA output to settle to its final value before being sampled. The conversion is then performed and the parallel output is updated, after a 2.5 cycle pipeline delay, on the rising edge of RSTCCD. The pipeline delay of the entire XRD9855/XRD9856 is 4 clock cycles.

The internal reference values are set by a resistor divider between V_{DD} and GND. To enable the internal reference, connect V_{RTO} to V_{RT} and connect V_{RBO} to V_{RB}. To maximize the performance of the XRD9855/XRD9856, the internal references should be used and decoupled to GND. Although the internal references have been set to maximize the performance of the CDS/PGA channel, some applications may require other reference values. To use external references, drive the V_{RT} pin directly with the desired voltage. Connect V_{RB} to V_{RBO}. Do not drive V_{RB} directly. The ADC parallel output bus is equipped with a high impedance capability, controlled by $\overline{OE}$. The outputs are enabled when $\overline{OE}$ is low.

Automatic Offset Calibration, Offset [7:0]

To get the maximum color resolution and dynamic range, this part uses a digital controlled offset calibration system to compensate for external offset in the CCD signal as well as internal offsets of the CDS, PGA and ADC.

The calibration is performed every frame when the CCD outputs the Optical Black pixels, please see the section on Frame Timing. The Calibration logic compares the ADC output to the value stored in the serial port offset register, and increments or decrements the offset adjust DAC to make the ADC code equal to the code in the offset register. The first adjustment requires 8 pixels, then 6 pixels for subsequent adjustments. The offset register is 8 bits wide. Two MSBs set to 00 are added when compared to the 10-bit ADC code. After power-up the part may require up to 264 adjustments to converge on the proper offset. These adjustments can be made over many lines or frames. For example, with 20 optical black pixels per line, the calibration will make 3 adjustments per line, and initial convergence will require at most 88 lines.



Graph 1. XRD9855 Typical Vdrk (CCD Offset) Calibration Range @ 25°C

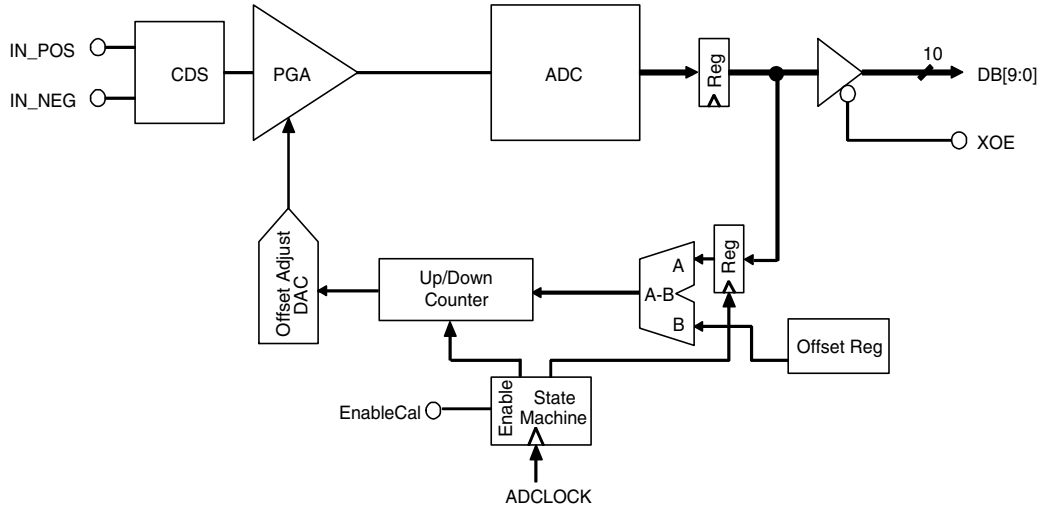


Figure 5. Automatic Offset Calibration Loop

Manual Global Offset, V [1:0]

In some systems the black level offset can be larger than the Automatic Offset Calibration Range. The XRD9855/XRD9856 provide a user programmable global offset adjustment which adds to the automatic offset calibration. The global offset is applied at the PGA input, so it's input referred value does not change with PGA gain code, see *Figure 6*. The magnitude of the global offset is controlled by bits V[1:0] in the mode register. (See *Table 1*.)

V[1]	V[0]	Offset
0	0	0mV
0	1	25mV (default)
1	0	50mV
1	1	75mV

Table 1. Manual Global Offset Programming

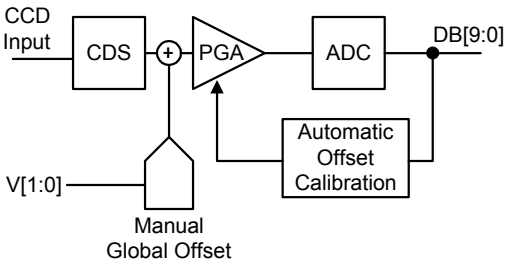


Figure 6. Manual Global Offset & Automatic Offset Calibration

Serial Interface

A three wire serial interface, (LOAD, SCLK, and SDI), is used to program the PGA gain register, the Calibration offset register, the Mode control register, and the Aperture delay register. The shift register is 10 bits long. The first two bits loaded are the address bits that determine which of the four registers to update. The following eight bits are the data bits (MSB first, LSB last). When LOAD is high SCLK is internally disabled. Since SCLK is gated by LOAD, SCLK can be a continuously running clock signal, but this will increase system noise. To enable the shift register the LOAD pin must be pulled low. The data at SDI is strobed into the shift register on the rising edges of SCLK. When the LOAD signal goes high the data bits will be written to the register selected by the address bits (see *Figure 7*).

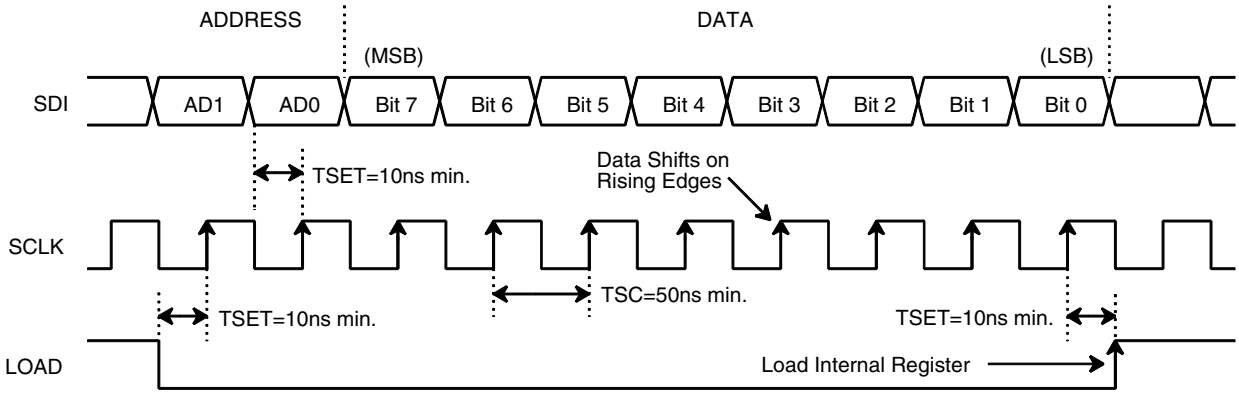


Figure 7. Serial Port Timing Diagram

	Address		Data							
Name	**AD1**	**AD0**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
Gain	0	0	Gain[7]	Gain[6]	Gain[5]	Gain[4]	Gain[3]	Gain[2]	Gain[1]	Gain[0]
Offset	0	1	Offset[7]	Offset[6]	Offset[5]	Offset[4]	Offset[3]	Offset[2]	Offset[1]	Offset[0]
Mode	1	0	V[1]	V[0]	M3	M2	Test3	Test2	M1	Reset
Delay	1	1	Dp[2]	Dp[1]	Dp[0]	Dd[2]	Dd[1]	Dd[0]	Dr[1]	Dr[0]

Table 2. Serial Interface Register Address Map

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Gain [7:0]							
0 0 0 0 0 0 0 0 - minimum gain (6dB) *							
1 1 1 1 1 1 1 1 - maximum gain (38 dB)							

Table 3. Gain Register Bit Assignment

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Offset [7:0]							
0 0 0 0 0 0 0 0 - do not use							
0 0 0 0 0 0 0 1 - do not use							
0 0 0 0 0 0 1 0 - minimum offset code							
0 0 0 0 1 0 0 0 - default offset code, typical offset code 00100000							
0 0 1 1 1 1 1 1 - maximum offset code							

Table 4. Offset Register Bit Assignment

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
V[1:0]		M3	M2	Test3	Test2	M1	Reset
0 0 - 0mV offset 0 1 - 25mV offset* 1 0 - 50mV offset 1 1 - 75mV offset		0 - Clamp only* 1 - Clamp & Cal	0 - RSTCCD* 1 - no RSTCCD	0 - TestVin off* 1 - TestVin on	0 - test off* 1 - factory test	0 - auto detect* 1 - manual	0 - normal* 1 - reset

Table 5. Mode Register Bit Assignment

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Dp[2:0]			Dd[2:0]			Dr[1:0]	
0 0 0 - SHP min delay * 1 1 1 - SHP max delay			0 0 0 - SHD min delay * 1 1 1 - SHD max delay			0 0 - RSTCCD min delay * 1 1 - RSTCCD max delay	

Table 6. Delay Register Bit Assignment

Note:

** Indicates default value*

SHP, SHD and RSTCCD Signals, M2 = 0

The SHP input to the XRD9855/XRD9856 determines when the Black level of each pixel is sampled. For CLK_POL=high timing mode, the black level is sampled on the falling edge of SHP. For CLK_POL=low timing mode, the black level is sampled on the rising edge of SHP.

The sampling edge of SHP should be positioned so that it samples the pixel black level at a stable and repeatable point. The black level should be sampled after the CCD output has had time to settle from the reset pulse and before the output transitions to the video level (see *Figure 8*). Aperture delay T_{BK} needs to be taken into consideration when positioning the sampling edge of SHP (see *Figure 8*). This aperture delay is the time from the sampling edge of SHP to the time the pixel black level is actually sampled by the CDS. The correct positioning of SHP will be 6-7 ns prior to where the black level has adequately settled. This is typically just before the CCD signal starts the transition to the video level.

The SHD input to the XRD9855/XRD9856 determines when the Video level of each pixel is sampled. For CLK_POL=high timing mode, the video level is sampled on the falling edge of SHD. For CLK_POL=low timing mode, the video level is sampled on the rising edge of SHD.

The sampling edge of SHD should be positioned so that it samples the pixel video level at a stable and repeatable point. The video level should be sampled after the CCD output has settled from the black level and before the output transitions to the reset pulse. Aperture delay T_{VD} needs to be taken into consideration when positioning the sampling edge of SHD (see *Figure 8*). This aperture delay is the time from the sampling edge of SHD to the time the pixel video level is actually sampled by the CDS. The correct positioning of SHD will be 5-6 ns prior to where the video level has adequately settled.

RSTCCD is intended to overlap the reset pulse of each pixel. This is intended to eliminate the reset pulse transients from getting into the CDS circuitry. Positioning of the RSTCCD signal so that it overlaps the CCD signal reset pulse is not always practical due to the timing generators being used or the frequency at which the CCD is running. The most critical thing to remember for RSTCCD is that it can not be high when sampling either the black level or video level.

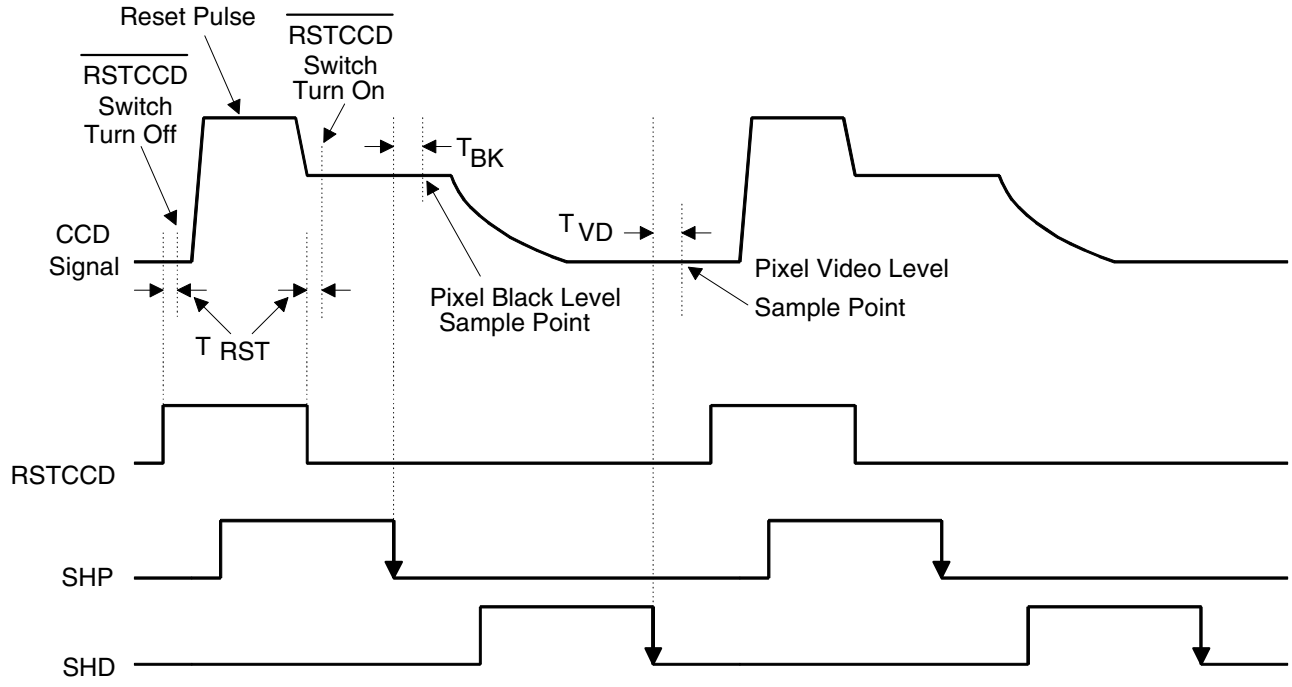


Figure 8. CDS Timing Diagram (CLK_POL = 1, M2 = 0)

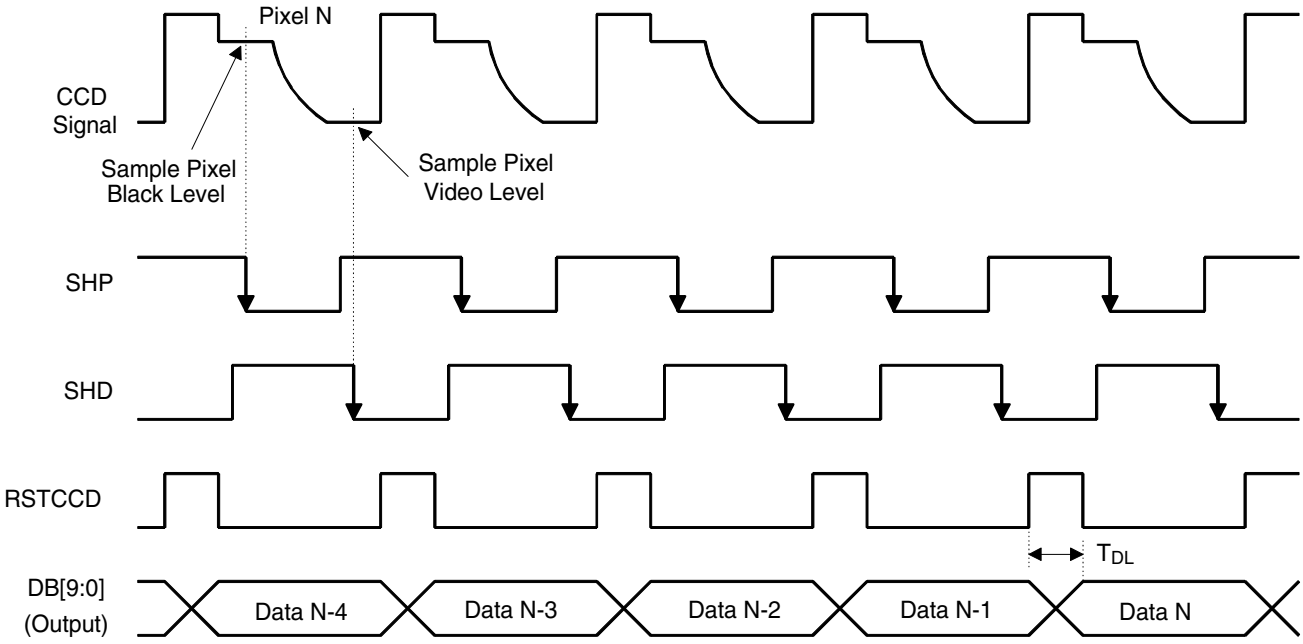


Figure 9. Conversion Timing Diagram Showing Pipeline Delay (CLK_POL = 1, M2 = 0)

CDS Clock Polarity

The CLK_POL pin is used to determine the polarity of the CDS clocks (SHD, SHP, CLAMP). See *Figures 10 & 11, and Tables 7 & 8.*

Event	Action
↑RSTCCD	Disconnect CDS Inputs from Reset Noise
↓RSTCCD	Connect CDS Inputs and Track Black Level
↓SHP	Hold Black Level and Track Video Level
↓SHD	Hold Video Level
↑SHP/SHD	No Action
Clamp High	Activate DC Restore Clamp
Enable_Cal High	Activate Offset Calibration

Table 7. Timing Event Description Table Valid for CLK_POL=1, M2=0

Event	Action
↑RSTCCD	Disconnect CDS Inputs from Reset Noise
↓RSTCCD	Connect CDS Inputs and Track Black Level
↑SHP	Hold Black Level and Track Video Level
↑SHD	Hold Video Level
↓SHP/SHD	No Action
Clamp Low	Activate DC Restore Clamp
Enable_Cal High	Activate Offset Calibration

Table 8. Timing Event Description Table Valid for CLK_POL=0, M2=0

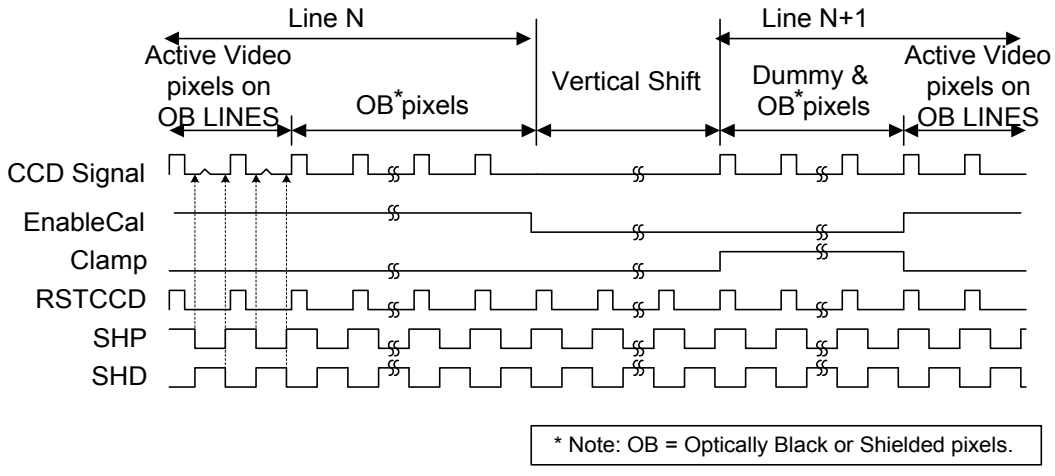
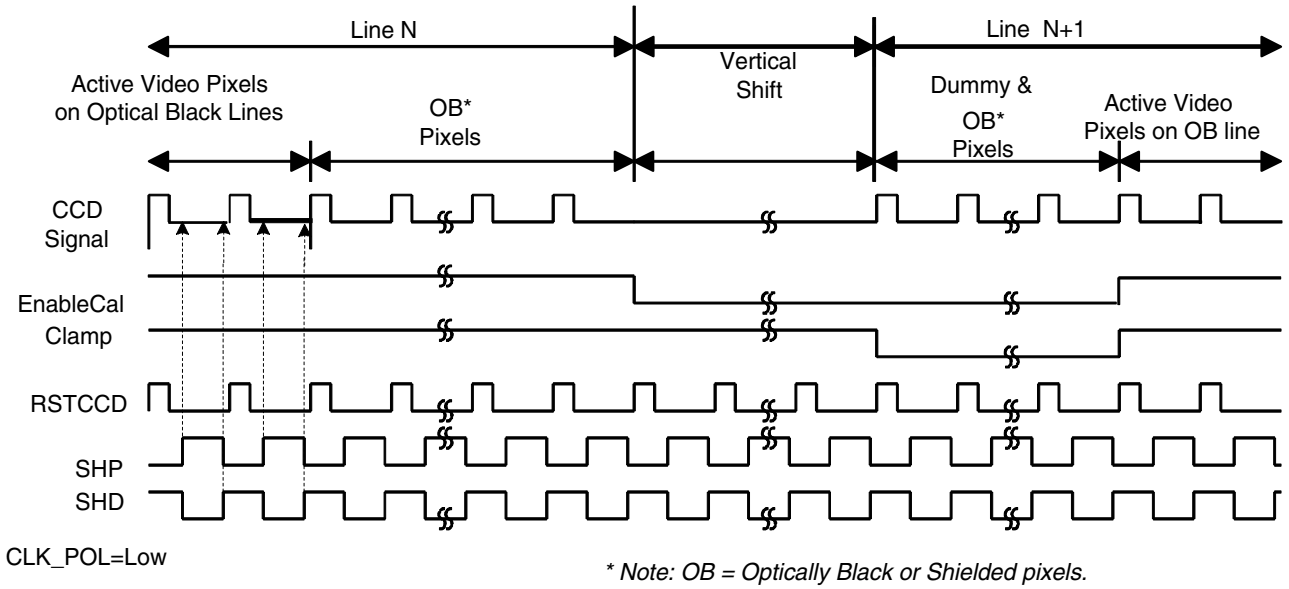


Figure 10. CCD Line Timing, CLK_POL= 1, M2 = 0



** Note: OB = Optically Black or Shielded pixels.*

Figure 11. CCD Line Timing with CLK_POL = 0, M2 = 0

No RSTCCD Pulse Timing, M2 = 1

To help simplify the timing required to drive the XRD9855/XRD9856 we have included a timing mode which does not require an active signal for RSTCCD. To use this timing, bit M2 in the timing mode register must be set high.

In this timing mode, RSTCCD must be kept low. No changes are required for the timing of the SHP and SHD signals. The polarity of SHP, SHD and Clamp are still controlled by the CLK_POL pin. The digital outputs change on the sampling edge of SHD (see *Figure 12*). This mode can be used with both the XRD4460 and XRD9853 compatible timing as described in the Line Timing section. Data output DB[9:0} is delayed as SHD is delayed with the delay feature AD[1:0] = [1,1].

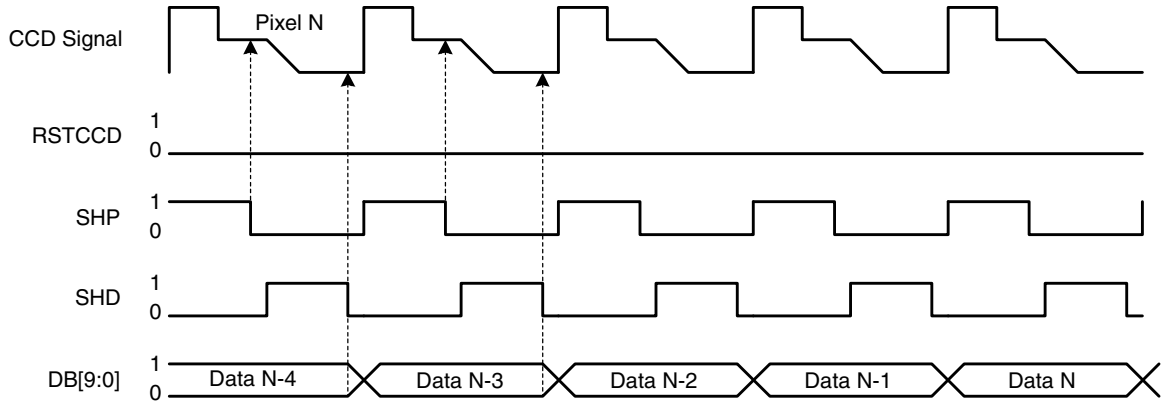


Figure 12. Timing for no RSTCCD Pulse, M2=1 & CLK_POL=1, RSTCCD=0

Programmable Aperture Delays Dp[2:0], Dd[2:0], Dr[1:0]

To help fine tune the pixel timing, the XRD9855/XRD9856 allows the system to adjust the aperture delays associated with SHP (T_{BK}), SHD (T_{VD}) and RSTCCD (T_{RST}) by programming the Aperture Delay serial port register. On power up these three aperture delays are set to their minimum values.

The SHP aperture delay is set by bits Dp[2:0]. Each LSB adds approximately 2ns of delay. The SHD aperture delay is set by bits Dd[2:0]. Each LSB adds approximately 2ns of delay. The RSTCCD aperture delay is set by bits Dr[1:0]. Each LSB adds approximately 4ns of delay.

Dp[2]	Dp[1]	Dp[0]	SHP Aperture Delay T_{BK} (typ)
0	0	0	6ns (default)
0	0	1	8ns
0	1	0	10ns
0	1	1	12ns
1	0	0	14ns
1	0	1	16ns
1	1	0	18ns
1	1	1	20ns

Table 9. Programmable SHP Delays

Dd[2]	Dd[1]	Dd[0]	SHD Aperture Delay T_{VD} (typ)
0	0	0	5ns (default)
0	0	1	7ns
0	1	0	9ns
0	1	1	11ns
1	0	0	13ns
1	0	1	15ns
1	1	0	17ns
1	1	1	19ns

Table 10. Programmable SHD Delays

Dr[1]	Dr[0]	RSTCCD Aperture Delay T_{RST} (typ)
0	0	3ns (default)
0	1	7ns
1	0	11ns
1	1	15ns

Table 11. Programmable RSTCCD Delays

Line Timing with Frame Calibration

At the beginning and/or end of every CCD frame there are a number of Optical black lines. The XRD9855/XRD9856 uses the output from these pixels for the DC Restore Clamp and Black Level Offset Calibration functions. These functions are controlled by the Clamp and/or EnableCal pins.

The XRD9855/XRD9856 is designed to be compatible with the Clamp Only timing of the XRD4460 or the Clamp & EnableCal timing of the XRD9853. On power up the chip will automatically detect which timing is being used and make the necessary internal adjustments. If EnableCal is high when Clamp is active, then "Clamp Only" timing is selected (M3=0). If EnableCal is low when Clamp is active, then "Clamp & Cal" timing is selected (M3=1). If required, the automatic detection function can be disabled through the serial port, and the chip can be forced into one of the two timing modes by programming mode register bits M3 & M1. Frame clibration however, can only be used with m3=0.

To maximize dynamic range in the dark areas of an image the PGA black level output must be equal to the bottom reference voltage of the ADC. This ensures that a dark pixel input corresponds to a desired minimum code output from the XRD9855 and XRD9856.

The XRD9855 and XRD9856 use the Optically Black (OB) pixels on a CCD array to calibrate for itself and the CCD. Figure 13 shows the outline of a typical CCD. The shaded region on the outside of the array indicates the position of the optically black (OB) pixels. The center region indicates the position of the active pixels used for an image.

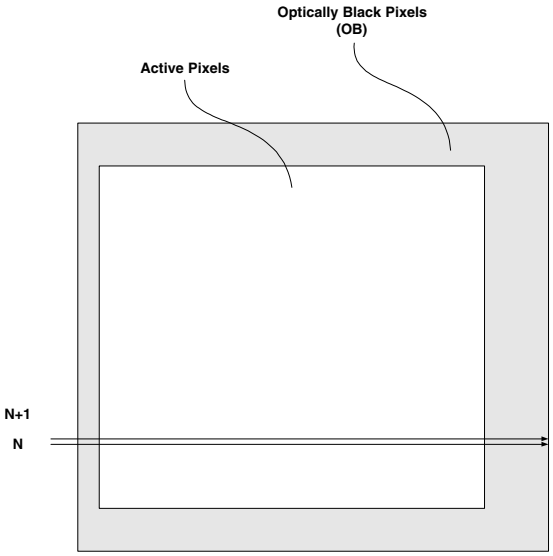


Figure 13. Typical Outline of an Area Array CCD.

The CCD has many OB pixels available for use in calibration. Some are available at the start and end of each line while whole lines of OB pixels are available at the top and bottom of the array.

The XRD9855 and XRD9856 take advantage of the large number of OB pixels available at the top and bottom of the CCD array to perform calibration before any active pixels are processed.

The XRD9855 and XRD9856 use a digital feedback loop to achieve auto-calibration. The output of the ADC and a desired dark code programmed in the offset register are compared during the OB pixel output from the CCD. The recommended offset register value is 32 decimal. The difference determines whether the offset adjustment DAC increments or decrements. This adjusts the offset of the PGA to achieve the desired ADC output code for a dark pixel input.

The first adjustment requires 8 cycles of SHP/SHD clocks but every subsequent adjustment requires only 6 cycles: 1 cycle for CDS, 3 cycles for A/D conversion, 1 cycle for logic, and 1 cycle for DAC update, see Figure 14. When Enable_Cal pin is low, the offset calibration logic is disabled, and the current state of the offset DAC is held constant.

The XRD9855 and XRD9856 calibration time depends on the calibration method and the number of OB pixels available. The time required to achieve calibration, in frame calibration, depends on the number of OB pixels present in each line.

Using Frame calibration, calibration can be achieved after several lines depending upon the number of OB pixels at the top or bottom of an array. Enable_Cal must be generated by the timing generator to properly frame the optical black lines.

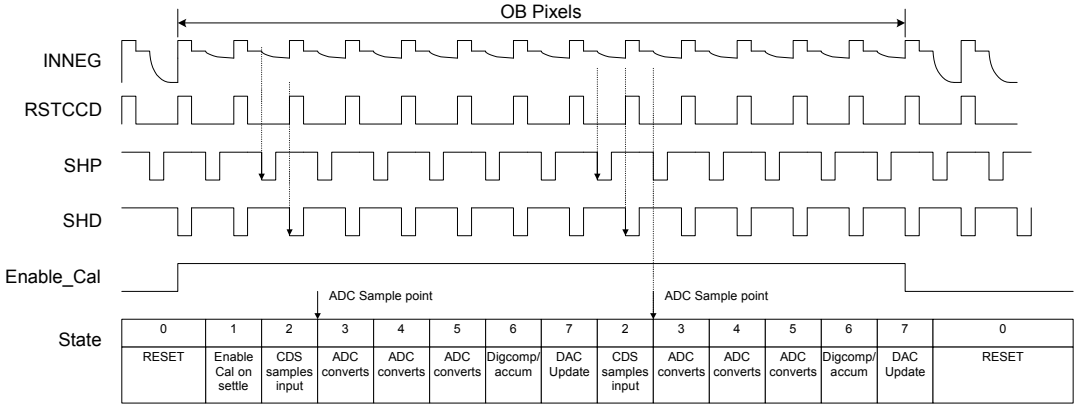


Figure 14. XRD9855 and XRD9856 Offset Calibration Timing, M3 = 1

Frame calibration uses the OB *lines* available at the start and end of the array, see the dark shaded regions at the top and bottom of Figure 15, to perform its auto-calibration.

The dark shaded regions of Figure 15 are the OB lines at the start and end of the CCD array. Typically, these OB lines are the largest blocks of OB pixels available on the array. Using these areas will allow the XRD9855 and XRD9856 to achieve calibration before any active pixels are processed. This means that the XRD9855 and XRD9856 can achieve calibration for the very first frame if OB lines are used for calibration at the start of the array.

The timing needed for Frame Calibration Mode is shown in Figure 16. In Frame Calibration Mode, Enable_Cal needs to be active during the OB line output from the CCD. Enable_Cal gates the XRD9855 and XRD9856's auto-calibration logic and must never be high when CLAMP is active. Clamp still needs to be active once a line, either during start of line or end of line OB pixels.

Frame calibration is useful for applications where fast calibration is needed. With frame calibration, the XRD9855 and XRD9856 can achieve calibration before the first frame is started.

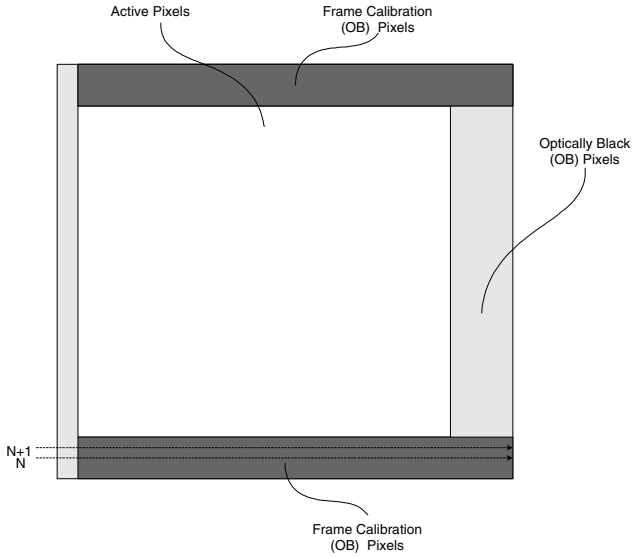


Figure 15. OB Lines Used For Frame Calibration on a Typical CCD Array

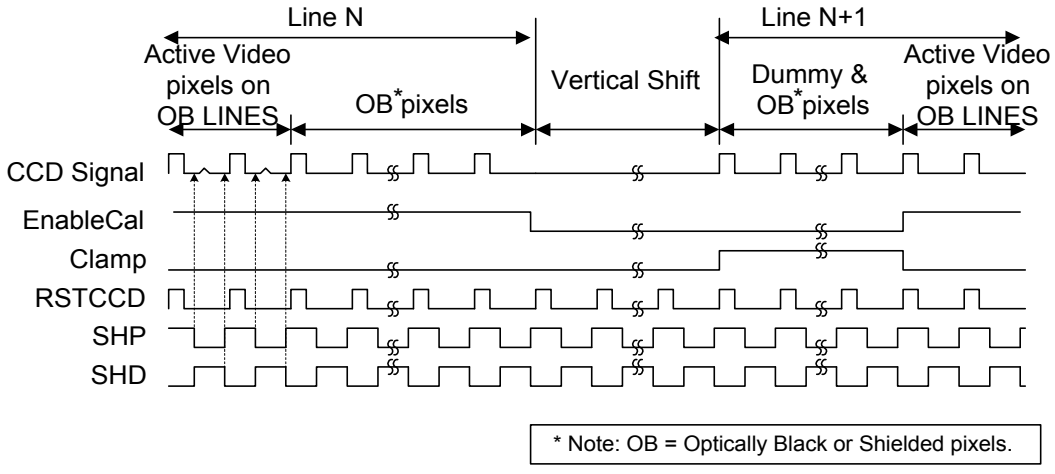
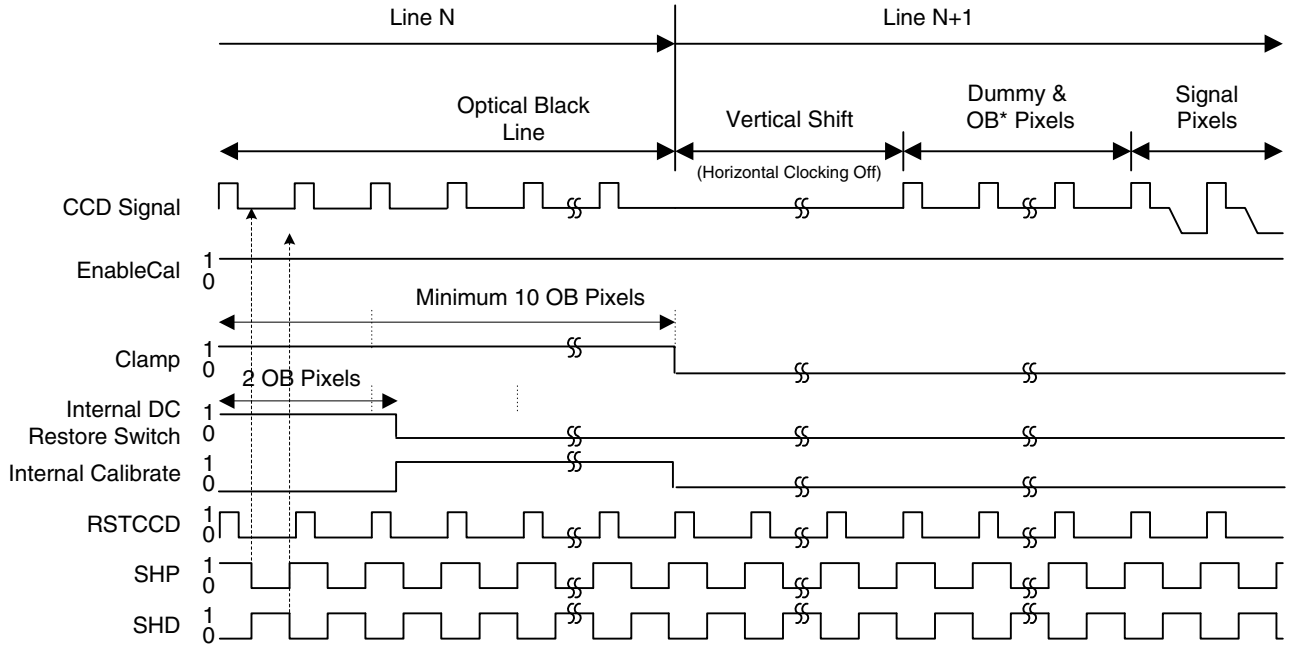


Figure 16. Frame Calibration Mode Timing, CLK_POL= High

Clamp Only Timing (XRD4460 compatible)
M1=1, M3=0, NOT RECOMMENDED

In this mode EnableCal is held high, and Clamp is activated during the Optical Black pixels. While this mode is available, it is not recommended for best performance. This timing does not perform frame calibration.

The Clamp signal is used to trigger a one-shot which controls the internal DC restore switch and the calibration logic. The DC restore switch is turned on for two pixels after Clamp is activated. Then the Calibration logic is enabled and runs until Clamp is deactivated. The chip can be forced into this timing mode by programming the Mode control register bits M1=1 and M3=0.



* Note: OB = Optically Black or Shielded pixels.

Figure 17. Clamp Only Line Timing
CLK_POL=1, EnableCal=1, M1=1, M3=0, M2=0

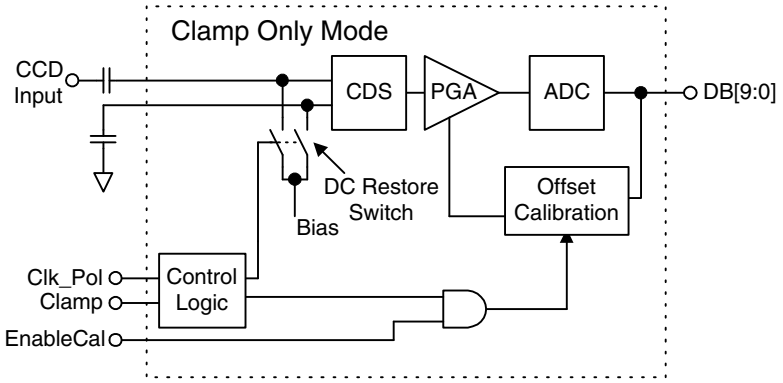


Figure 18. Clamp Only Mode (XRD4460 Compatible)
M1=1, M3=0

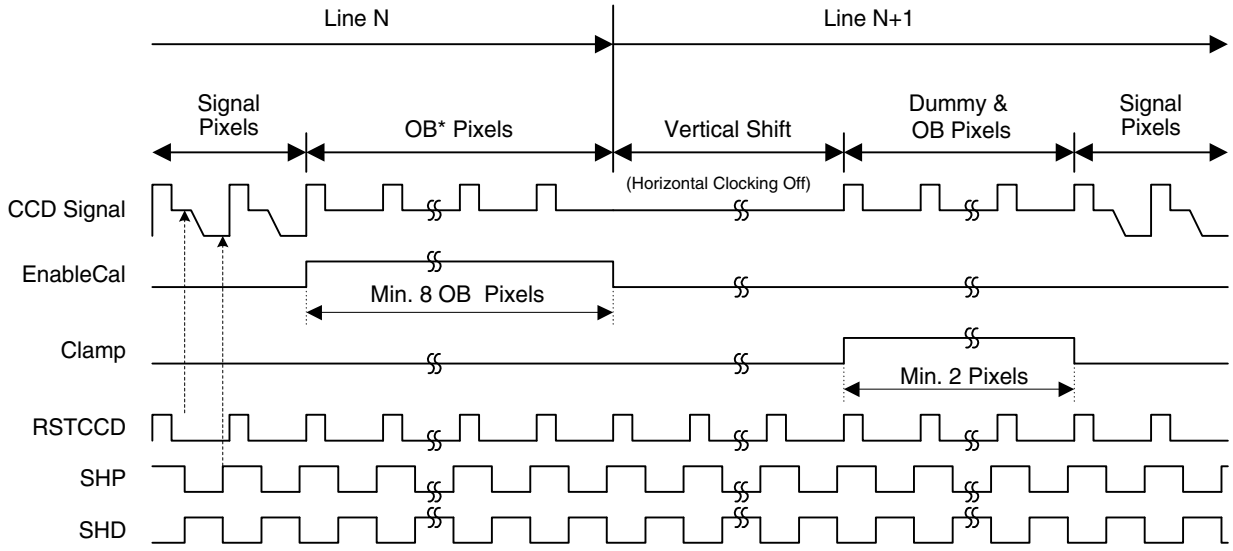
Clamp & EnableCal Timing (XRD9853 Compatible) M1=1, M3=1

In this mode EnableCal must be active during the large number of Optical Black pixels (usually at the end of each CCD line or at the start of a frame), Clamp should be active during the Dummy pixels (usually at the beginning of each CCD line).

The EnableCal pin (always active high) directly controls the calibration logic.

The Clamp pin (polarity determined by CLK_POL) controls only the DC restore switch at the CDS input. EnableCal and Clamp must not be active at the same time. Clamp must be used every line.

The chip can be forced into this timing mode by programming the Mode control register bits M1=1 and M3=1.



* Note: OB = Optically Black or Shielded Pixels.

Figure 19. Clamp & EnableCal Timing, CLK_POL=1, M1=1, M3=1, M2=0

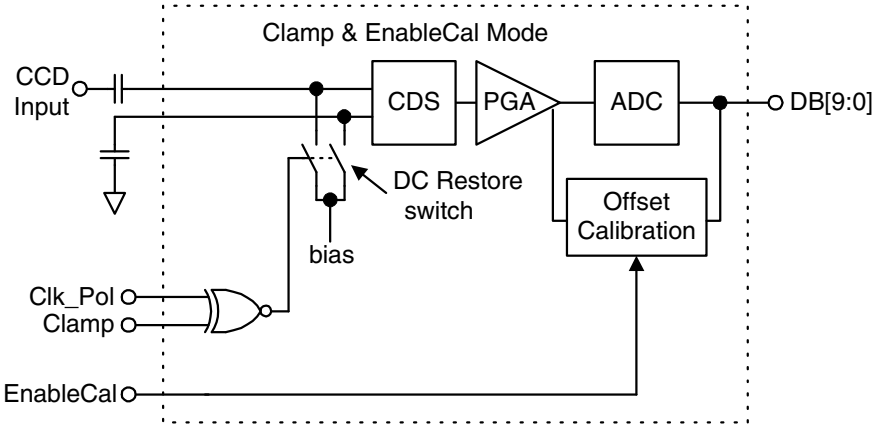


Figure 20. Clamp & Enable Cal Mode (XRD9853 Compatible), M1=1, M3=3

Stand-by Mode (Power Down)

The $\overline{\text{STBY1}}$ and $\overline{\text{STBY2}}$ pins are used to put the chip into the Stand-by or Power down mode. In this mode all sampling and conversion stops, The digital outputs are put into the high impedance mode, and the power supply current will drop to less than 50µA.

For most applications $\overline{\text{STBY1}}$ and $\overline{\text{STBY2}}$ should be connected together and treated as a single control pin. If an application uses the TestVin pin to access the PGA output or the ADC input then $\overline{\text{STBY1}}$ and $\overline{\text{STBY2}}$ must be separately controlled, see the truth table below.

STBY2	STBY1	CDS/ PGA	ADC	Clock Inputs	Digital Outputs
0	0	Off	Off	Off	High-z
1	0	On	Off	On	High-z
0	1	Off	On	On	On
1	1	On	On	On	On

Table 12. Stand-by Truth Table

Chip Reset

The chip has an Internal Power-On-Reset function to ensure all internal control registers start up in a known state. Pulling the Reset pin high or writing a logic 1 to the Mode Registers reset bit will also reset the chip to the Power-up default conditions.

Register	Default	Notes
Gain[7:0]	00000000	minimum gain
OS[7:0]	00001000	code 08 hex
V[1:0]	01	25 mV offset
M3	0	Clamp only
M2	0	RSTCCD required
M1	0	Automatic timing detect On
Test3	0	Test modes off
Test2	0	Test modes off
Reset	0	reset bit will reset itself
Dp[2:0]	000	minimum delay
Dd[2:0]	000	minimum delay
Dr[1:0]	00	minimum delay

Table 13. Reset Conditions

Using TestVin (Pin 20)

The TestVin pin allows access to the input of the ADC, or it can be used to monitor the CDS/PGA output. The TestVin pin accesses the ADC input node through switch S1 (see *Figure 18*). This switch is controlled by Bit3 of the serial port Test register. When the TEST3 bit of the mode register is high, switch S1 is “ON” and the TestVin pin can be used to access the ADC input/PGA output. When the TEST3 bit of the mode register is low, switch S1 is “OFF” and the TestVin pin is disconnected from the ADC input/PGA output.

To use TestVin as an auxiliary ADC input force STBY2=low and STBY1=high. This will disable the CDS/PGA and leave the ADC operating. If M2=0, the ADC clock is generated from RSTCCD and SHP (*See Figure 19*). If M2=1, the ADC clock is generated from SHP & SHD (*See Figure 20*).

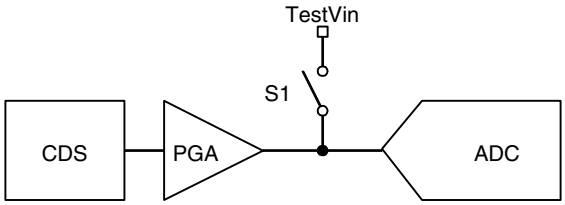


Figure 21. Using TestVin to Access PGA Output & ADC Input

Mode Reg.	AD1	AD0	V[1]	V[0]	M3	M2	Test3	Test2	M1	Reset
TestVin	1	0	0	0	0	1	1	0	0	0
Normal	1	0	0	0	0	1	0	0	0	0

Table 14. Serial Port Data to Use TestVin

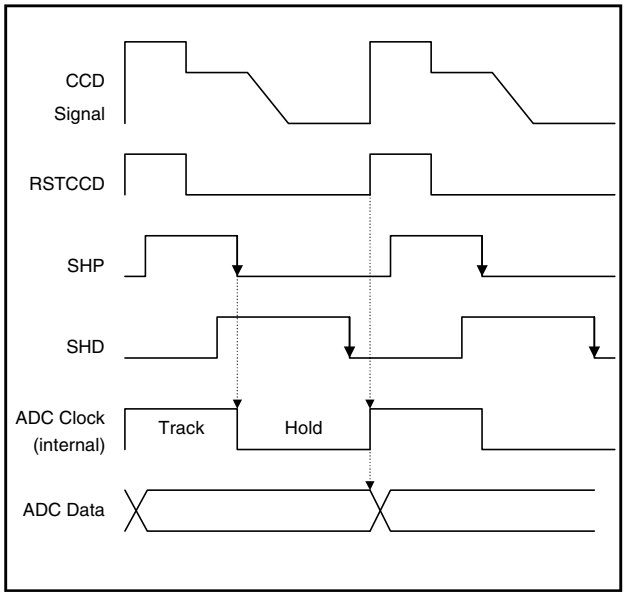


Figure 22. ADC Clock Generation, CLK_POL=1, M2=0

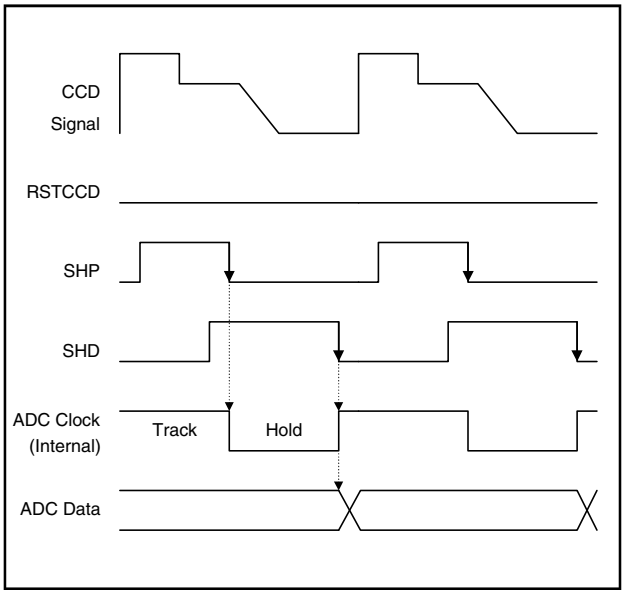


Figure 23. ADC Clock Generation, CLK_POL=1, M2=1

Digital Output Power Supplies

The DV_{DD} and DGND pins supply power to the digital output drivers for pins DB[9:0], UNDER, and OVER. DV_{DD} is isolated from V_{DD} so it can be at a voltage level less than or equal to V_{DD}. This allows the digital outputs to interface with advanced digital ASICs requiring reduced supply voltages. For example V_{DD} can be 5.0 or 3.3V, while DV_{DD} is 2.5V.

Power Supply Sequencing

There are no power supply sequencing issues if DV_{DD} and V_{DD} of the XRD9855/XRD9856 are driven from the same supply. When DV_{DD} and V_{DD} are driven separately, V_{DD} must come up at the same time or before DV_{DD}, and go down at the same time or after DV_{DD}. If the power supply sequencing in this case is not followed, then damage may occur to the product due to current flow through the source-body junction diodes between DV_{DD} and V_{DD}. An external diode (5082-2235) layed out close to the converter from DV_{DD} to V_{DD} prevents damage from occurring when power is cycled incorrectly.

Note: *V_{DD} must be greater than or equal to DV_{DD} or the source-body diodes will be forward based.*

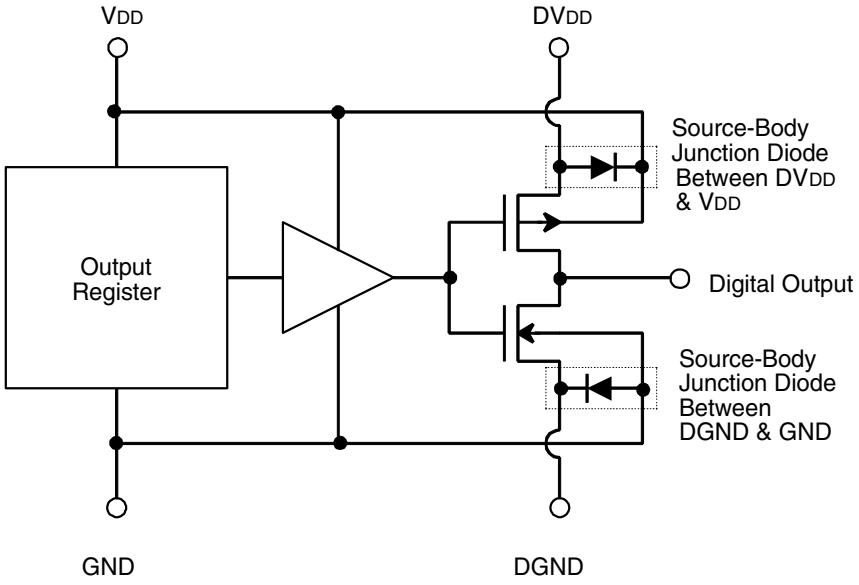


Figure 24. DV_{DD} & DGND Digital Output Power Supplies, $V_{DD} \geq DV_{DD}$

General Power Supply and Board Design Issues

All of the GND pins, including DGND, should be connected directly to the analog ground plane under the XRD9855/XRD9856. The V_{DD}'s should be supplied from a low noise, well filtered regulator which derives the power supply voltage from the CCD power supply. All of the V_{DD} pins are analog power supplies and should be locally decoupled to the nearest GND pin with a 0.1µF, high frequency capacitor. DV_{DD} is the power supply for the digital outputs and should be locally decoupled. DV_{DD} should be connected to the same power supply network as the digital ASIC which receives data from the XRD9855/XRD9856.

In general, all traces leading to the XRD9855/XRD9856 should be as short as possible to minimize signal crosstalk and high frequency digital signals from feeding into sensitive analog inputs. The two CCD inputs, In_Pos and In_Neg, should be routed as fully differential signals and should be shielded and matched. Efforts should be made to minimize the board leakage currents on In_Pos and In_Neg since these nodes are AC coupled from the CCD to the XRD9855/XRD9856. The digital output traces should be as short as possible to minimize the capacitive loading on the output drivers (see *Figure 25*)

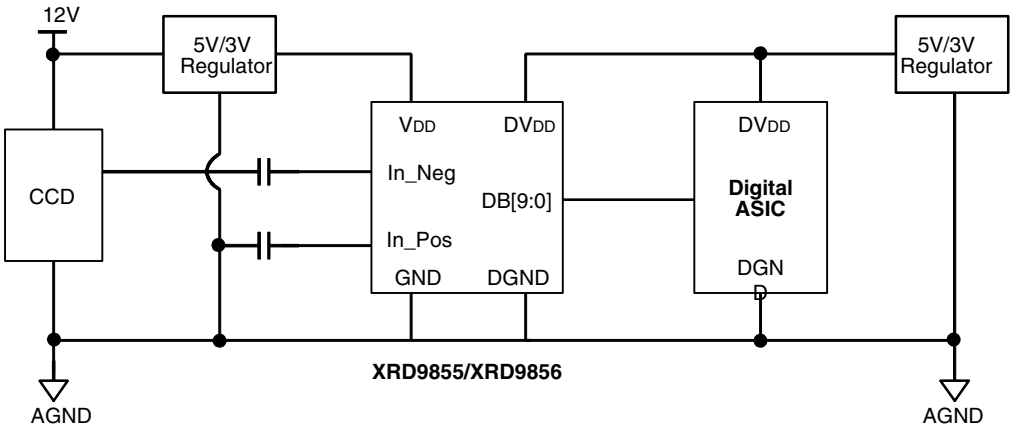


Figure 25. XRD9855/XRD9856 Power Supply Connections

Application Note

If increasing the PGA Gain to code 128 (80h) or higher causes a larger than expected offset increase in the ADC digital output codes, the problem may be due to the limited Automatic Offest Calibration range. This problem may be solved by increasing the Global Offset code, V[1:0], in the Mode Register. The default is V[1:0] = 01 (binary). Try increasing to V[1:0] = 10, or V[1:0] = 11.

For additional information on the XRD9855 feaures:

- Auto-detect
- EnableCal & Clamp Line Timing
- Clamp Only Line Timing
- Digital Clibration Loop
- Dark Voltage Calibration Range

Please see Application Notes XRDAN109, XRDAN110, XRDAN112, XRDAN113 and XRDAN114.

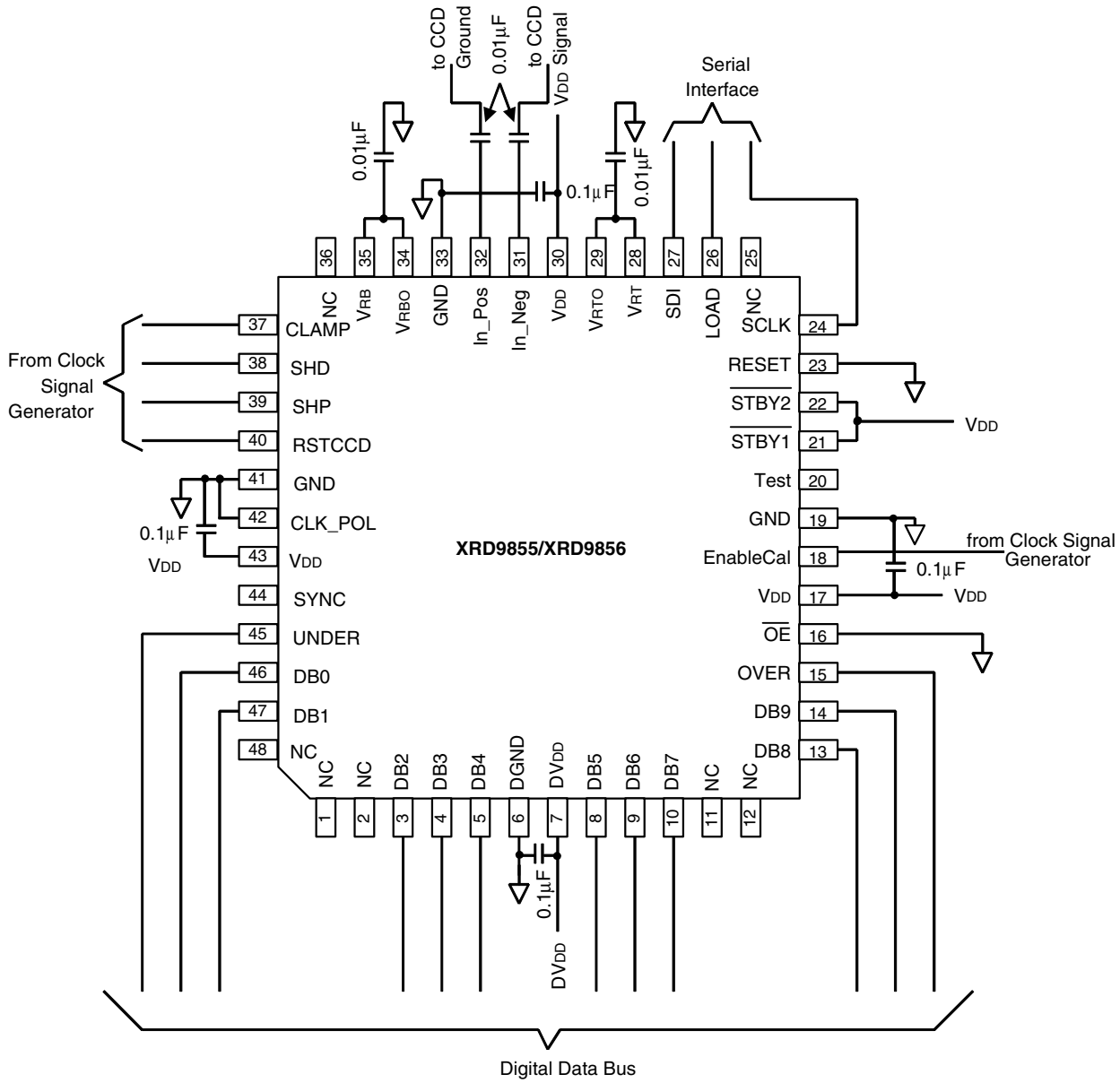


Figure 26. XRD9855/XRD9856 Application Schematic
CLK_POL=0

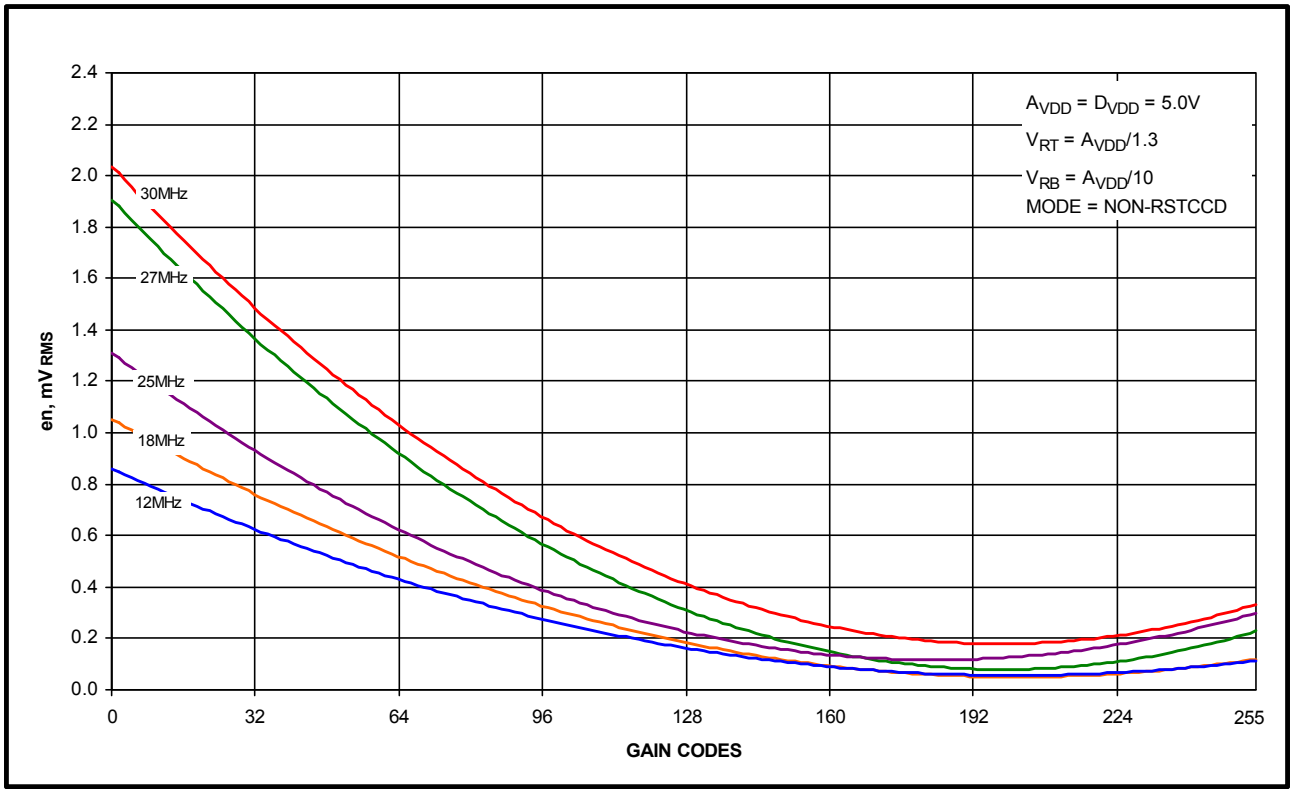


Figure 27. Input Reference Noise vs. PGA Gain Codes

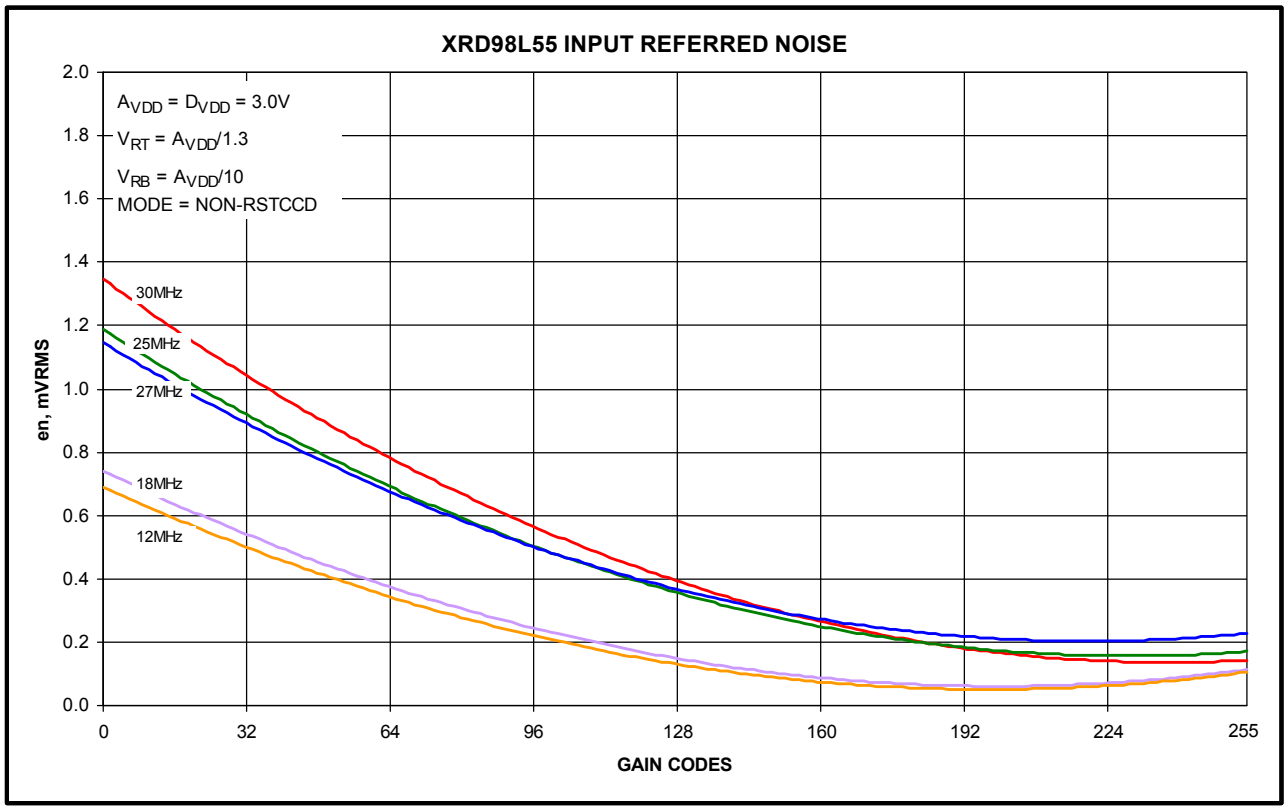
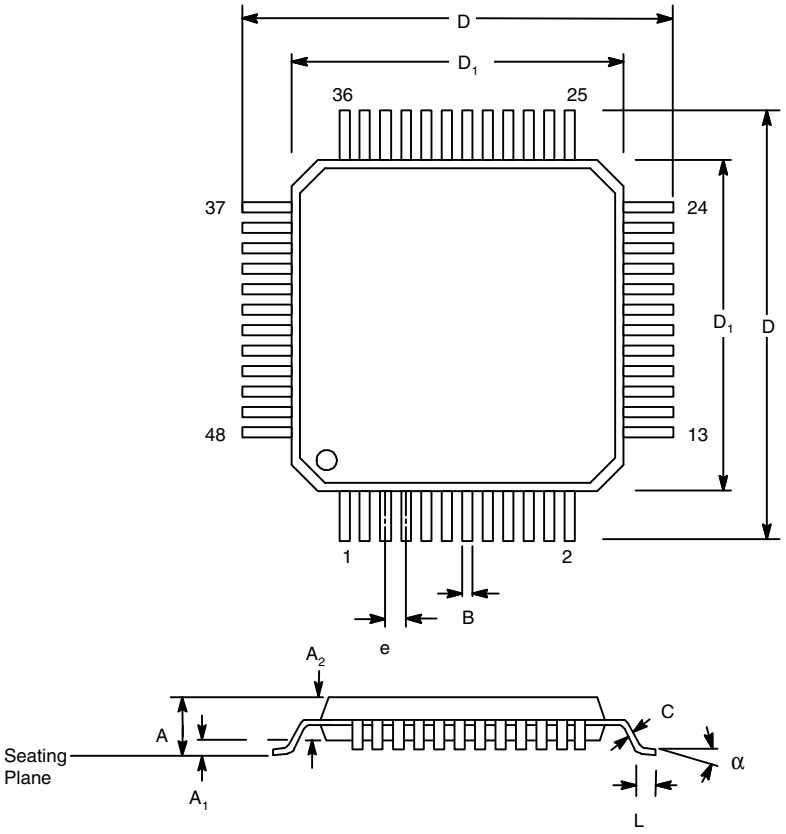


Figure 28. XRD98L55 Input Referred Noise

48 LEAD THIN QUAD FLAT PACK
(7 x 7 x 1.4 mm TQFP)
rev. 2.00



SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.055	0.063	1.40	1.60
A1	0.002	0.006	0.05	0.15
A2	0.053	0.057	1.35	1.45
B	0.007	0.011	0.17	0.27
C	0.004	0.008	0.09	0.20
D	0.346	0.362	8.80	9.20
D1	0.272	0.280	6.90	7.10
e	0.020 BSC		0.50 BSC	
L	0.018	0.030	0.45	0.75
a	0×	7×	0×	7×

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